SPECIFICATION AMENDMENTS

1. Please **replace** the **paragraph** which begins on **page 12, line 18**, with the following rewritten paragraph:

Referring now to Figure 2, in order to generate a positive charge in the body of the NMOS transistor of Figure 1, the gate voltage V_g and drain voltage V_d, as well as the source voltage, are initially zero. At time t_0, the gate voltage is brought to -1.5V and at time $t_0 + \Delta t_0$ (where Δt_0 can be greater than, less than or equal to zero), the drain voltage V_d is brought to -2V, while the source voltage remains at zero volts. By applying a negative voltage pulse to the gate 28 and a more negative voltage pulse to the drain 22, a concentration of negative charge forms in the body 20 in the vicinity of the gate 28, while a concentration of positive charge forms in the body 20 in the vicinity of insulating layer 12. At the same time, a conduction channel linking the source 18 and drain 22 forms in the body 20, allowing conduction of electrons between the source 18 and drain 22. This allows electrons to be attracted into the channel from the source 18 and/or drain 22.

2. Please **replace** the **paragraph** which begins on **page 13, line 6**, with the following rewritten paragraph:

The application of a negative voltage to the drain 22 relative to the source 18 as shown in Figure 2 generates electron-hole pairs by impact ionisation in the vicinity of the source 18. The holes accumulated in the floating body 20 create a positive charge.

3. Please **<u>replace</u>** the **paragraph** which begins on **page 13, line 9**, with the following rewritten paragraph:

The ~~drain~~ voltage V_d <u>applied to the drain 22</u> then returns at time t_1 to zero, and the ~~gate~~ voltage V_g <u>applied to the gate 28</u> returns to zero at $t_1 + \Delta t_1$ to remove the conductive channel between the source 18 and drain 22, the time interval $t_1 - t_0$ typically being between a few nanoseconds and several tens of nanoseconds, while Δt_1 is of the order of 1 nanosecond. It is also possible to create a positive charge in the body 20 by applying a positive ~~drain~~ voltage pulse <u>to the drain 22</u>, depending upon the voltages ~~of~~ <u>applied to</u> the source <u>18</u>, drain <u>22</u> and gate <u>28</u> relative to each other. It has been found in practice that in order to create a positive charge in the body <u>20</u>, the ~~drain~~ voltage <u>applied to the drain 22</u> must be switched back to zero <u>volts</u> before the ~~gate~~ voltage <u>applied to the gate 28 is switched back to zero volts</u>.

4. Please **<u>replace</u>** the **paragraph** which begins on **page 13, line 17**, with the following rewritten paragraph:

Referring now to Figure 3, a negative charge is generated in the body 20 by increasing the ~~gate~~ voltage V_g <u>applied to the gate 28</u> to +1V at t_0 while the <u>voltages applied to the</u> source <u>18</u> and drain <u>22</u> ~~voltages~~ are held at zero <u>volts</u>, then reducing the ~~drain~~ voltage V_d <u>applied to the drain 22</u> to -2V at time $t_0 + \Delta t_0$ while the ~~source~~ voltage <u>applied to the source 18</u> is held at zero <u>volts</u>. The ~~gate~~ voltage V_g <u>applied to the gate 28</u> and ~~drain~~ voltage V_d <u>applied to the drain 22</u> are then subsequently brought to zero

volts at times t_1 and $t_1 + \Delta t_1$ respectively, where Δt_1 can be positive or negative (or zero). The application of a positive voltage to the gate 28 relative to the voltages applied to the source 18 and drain 22 again causes the formation of a conductive channel between the source 18 and drain 22, as was the case with the formation of an excess positive charge as described above with reference to Figure 2. The positive voltage applied to the gate 28 also creates a concentration of negative charge in the body 20 in the vicinity of the gate 28, and a concentration of positive charge in that part of the body 20 which is remote from the gate 28, i.e., adjacent the insulating layer 12.

5. Please **replace** the **paragraph** which begins on **page 14, line 6**, with the following rewritten paragraph:

As a result of the application of the negative voltage to the drain 22, the body-drain junction is forward biased, as a result of which holes are conducted out of the body 20 to the drain 22. The effect of this is to create an excess of negative charge in the body 20. It should be noted that under these bias conditions the generation of holes by impact ionisation is fairly weak. Alternatively, a positive voltage pulse can be applied to the drain 22 and the gate 28, as a result of which the body-source junction is forward biased and the holes are removed from the body 20 to the source 18. In a similar way, instead of generating a negative charge in the body 20, a positive charge stored in the body 20 can be removed.

6. Please **<u>replace</u>** the **paragraph** which begins on **page 15, line 9**, with the following rewritten paragraph:

In order to operate the transistor of Figure 5a, the source is held at 0V, the ~~gate~~ voltage V_g <u>applied to the gate 128</u> is -1.5V and the ~~drain~~ voltage V_d <u>applied to the drain 122</u> is + 1V. This causes the tunnel effect at the interface of the body 120 and drain 122 as a result of the fact that the valence band B_v and conduction band B_c, represented schematically in Figure 5b, are distorted. Folding of these bands can be achieved by an electric field of the order of 1MV/cm, which results in electrons being extracted by the drain 122, while the associated holes remain in the body 120. This physical phenomenon is known as "GIDL" (Gate Induced Drain Leakage), described in greater detail for example in the article by Chi Chang et al "Corner Field Induced Drain Leakage in Thin Oxide MOSFETS", IEDM Technical Digest, Page 714, 1987.

7. Please **<u>replace</u>** the **paragraph** which begins on **page 18, line 23**, with the following rewritten paragraph:

Figure 8 shows a further embodiment of a transistor in which the voltage required to remove charge stored in the body <u>320</u> of the transistor is reduced. During discharging of the charged body <u>320</u>, pulses are applied to the drain <u>322</u> and to the gate <u>328</u> of the transistor so that the body/source or body/drain junction is biased in a forward direction. As a result, the majority carriers are removed from the charged floating body <u>320</u>, providing a decrease in channel current when the transistor is switched to its conductive state (see Figure 4).

8. Please **replace** the **paragraph** which begins on **page 19, line 5**, with the following rewritten paragraph:

The potential of the floating body 320 can be altered by adjusting the voltages applied to the transistor contacts, or by altering the body/source and/or body/drain and/or body/gate capacitances. For example, if the potential of the ~~transistor~~ drain 322 is positive compared to that of the source 318, the potential of the floating body 320 ~~potential~~ can be made more positive by increasing the capacitance between the drain 322 and the floating body 320. In the arrangement shown in Figure 8, the MOSFET has different doping profiles for the drain 322 and the source 318. In particular, a P+ doped region 330 is formed in the vicinity of the drain 322, which leads to an increased capacitance between the drain 322 and the floating body 320. This is manufactured by adding an implant on the drain side only, and by diffusing this implant before forming the source and drain implanted regions. An alternative is to increase the capacitive coupling between the drain 322 and the floating body 320 by using different geometries for the drain 322 and the source 318, as shown in Figure 9.

9. Please **replace** the **paragraph** which begins on **page 21, line 3**, with the following rewritten paragraph:

As pointed out above, the charge states of the body 20 of the transistor can be used to create a semiconductor memory device, data "high" states being represented by a positive charge ~~on~~ in the body 20, and data "low" states being represented by a negative or zero charge.

The data stored in the transistor can be read out from the memory device by comparing the source-drain current of the transistor with that of an uncharged reference transistor.